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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HENRY, MATTHEW ALLAN	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,594	UCHIDA, TOSHIYA	
	Examiner	Art Unit	
	Matthew A. Henry	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/17/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the data input-and-output unit described in Claims 7 and 15 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3 and 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Dreps.

Regarding Claim 1, Dreps discloses:

A data input circuit (Figure 4A, Item 332; commands are a type of data) comprising:

a clock signal supplying unit (Figure 3, Item 334) which supplies a clock signal (Figure 5A, Item 336) to a first data acquisition unit (Figure 5A, Item 502) and a second data acquisition unit (Figure 5A, Item 504);

a data input unit which receives a first data and a second data (Figure 3, Item 330), and supplies the first data and the second data (Figure 5A, Item 322) to a first data acquisition unit (Figure 5A, Item 502) and a second data acquisition unit (Figure 5A, Item 504);

said first data acquisition unit (Figure 5A, Item 502) which acquires said first data in response to a first edge of said clock signal (Column 7, Lines 48-51), where the first edge is one of a rising edge and a falling edge of the clock signal (Column 7, Lines 51-57);

and said second data acquisition unit (Figure 5A, Item 504) which acquires said second data in response to a second edge of said clock signal, where the second edge is an edge of the clock signal which is different from said first edge (Column 7, Lines 59-64).

Regarding Claim 2, Dreps discloses:

A data handling device (Figure 4A, Item 332) comprising:

a clock signal supplying unit (Figure 3, Item 334) which supplies a clock signal to a first data acquisition unit (Figure 5A, Item 502; commands are a type of data) and a second data acquisition unit (Figure 5A, Item 504);

a data input unit which receives a first data and a second data (Figure 3, Item 330), and supplies the first data and the second data to a first data acquisition unit (Figure 5A, Item 502) and a second data acquisition unit (Figure 5A, Item 504);

said first data acquisition unit (Figure 5A, Item 502) which acquires said first data in response to a first edge of said clock signal (Column 7, Lines 48-51), where the first edge is one of a rising edge and a falling edge of the clock signal (Column 7, Lines 51-57);

said second data acquisition unit (Figure 5A, Item 504) which acquires said second data in response to a second edge of said clock signal, where the second edge is an edge of the clock signal which is different from said first edge (Column 7, Lines 59-64);

and a processing unit which performs processing in accordance with said first data and said second data (Figure 3, Items 302 or 304).

Regarding Claim 3, Dreps discloses:

a processing unit which performs processing in accordance with said first data and said second data (Figure 3, Items 302 or 304).

It is therefore inherent to the operation of the system that:

said processing unit starts said processing when the processing unit receives said first data.

If the processing made by the unit is performed based upon the data received from the data input circuit, the reception of the first data from the input circuit will cause the processor to commence processing. If this were not the case, then the processing unit would not perform processing in accordance with said first data and second data.

Regarding Claim 8, Dreps discloses:

A data input circuit (Figure 4A, Item 332; commands are a type of data) comprising:

m data acquisition units (Figure 6A, Items 608, 602 and 605; the Items listed are a representative example of the m 'data acquisition units') which are provided corresponding to first to mth pieces of data, respectively, where m is an integer greater than one (Figure 6A, Items 604, 614, 624 and 634);

a clock signal supplying unit (Figure 3, Item 334) which supplies n clock signals respectively having different phases (Column 9, Lines 27-32) to said m data acquisition units, where n is an integer greater than one (Figure 6A, Items 605, 615, 625, 635);

and a data input unit which receives said first to mth pieces of data (Figure 3, Item 330), and supplies the first to mth pieces of data to said m data acquisition units (Figure 6A, Items 604, 614, 624, 634 and Label "Data from RX 330);

wherein each of the m data acquisition units acquires one of said first to mth pieces of data corresponding to said each of the m data acquisition units in response to one of m edges of said n clock signals corresponding to said one of the first to mth pieces of data (Column 9, Lines 23-25).

Regarding Claim 9, Dreps discloses:

A data handling device (Figure 4A, Item 332) comprising:

m data acquisition units (Figure 6A, Items 608, 602 and 605; the Items listed are a representative example of the m 'data acquisition units'; commands are a type of data) which are provided corresponding to first to mth pieces of data, respectively, where m is an integer greater than one (Figure 6A, Items 604, 614, 624 and 634);

a clock signal supplying unit (Figure 3, Item 334) which supplies n clock signals respectively having different phases (Column 9, Lines 27-32) to said m data acquisition units, where n is an integer greater than one (Figure 6A, Items 605, 615, 625, 635);

a data input unit which receives said first to mth pieces of data (Figure 3, Item 330), and supplies the first to mth pieces of data to said m data acquisition units (Figure 6A, Items 604, 614, 624, 634 and Label "Data from RX 330);

and a processing unit which performs processing in accordance with said first to mth pieces of data (Figure 3, Items 302 or 304);

wherein each of the m data acquisition units acquires one of said first to mth pieces of data corresponding to said each of the m data acquisition units in response to one of m edges of said n clock signals corresponding to said one of the first to mth pieces of data (Column 9, Lines 23-25).

Regarding Claim 10, Dreps discloses:

a processing unit which performs processing in accordance with said first to mth pieces of data (Figure 3, Items 302 or 304).

It is therefore inherent to the operation of the system that:

said processing unit starts said processing when the processing unit receives said first data.

If the processing made by the unit is performed based upon the pieces of data received from the data input circuit, the reception of the first data from the input circuit will cause the processor to commence processing. If this were not the case, then the processing unit would not perform processing in accordance with said first to mth pieces of data.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dreps.

Regarding Claim 6, Dreps discloses:

a data input unit which receives a first data and a second data, and supplies the first data and the second data to a first data acquisition unit and a second data acquisition unit,

said first data acquisition unit which acquires said first data in response to said first edge of said clock signal, and

said second data acquisition unit which acquires said second data in response to said second edge of said clock signal.

Dreps does not address the type of data being handled. It is well known in the art that a basic computer communicates three types of such information: address, control/command and data. Accordingly, it would have been obvious to a person of ordinary skill in the art at the time

of invention to apply the teachings of Dreps to all types of data, including address and command data to take advantage of the increased speed in data transfer.

Regarding Claim 14, Dreps does not disclose:

The data handling device according to claim 9, *further* comprising,

first to pth data acquisition units which are provided corresponding to first to pth pieces of data, respectively, where p is an integer greater than one, and

an data input unit which receives said first to pth pieces of data, and supplies the first to pth pieces of data to said first to pth data acquisition units,

wherein each of said first to pth data acquisition units acquires one of said first to pth pieces of data corresponding to said each of said first to pth data acquisition units in response to one of first to pth edges of said n clock signals corresponding to said one of the first to pth pieces of data.

Dreps does not address the type of data being handled. It is well known in the art that a basic computer communicates three types of such information: address, control/command and data. Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of invention to apply the teachings of Dreps to all types of data, including address and command data to take advantage of the increased speed in data transfer.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dreps in view of *Double Data Rate SDRAM*.

Regarding Claim 7, Dreps discloses:

a data input-and-output unit (Figure 5A, Items 510 and 512) which receives and outputs 2n bits of data in response to every rising edge of the clock signal.

Dreps does not disclose n bits of data being output or received on both the rising edge and the falling edge of the clock signal.

Double Data Rate SDRAM teaches:

Bandwidth may be doubled "by transferring data twice per cycle—on both the rising and falling edges of the clock signal." In other words, double the throughput of a bus may be output in a single clock period.

Faster data transfer is a fundamental goal in computer engineering. While doubling the bus width will double bandwidth, this article teaches that the same goal may be reached without increasing the cost of adding n more bus lines.

The disclosure of Dreps shows that 2n bits of data are output in one period of a clock signal. It would have been obvious to a person of ordinary skill in the art at the time of invention to modify Dreps in view of *Double Data Rate SDRAM* because it would have afforded the same amount of data throughput but at the savings of n data lines.

7. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dreps in view of Marhsall.

Regarding Claim 4, Dreps does not disclose:

The detection of an errant data received by a processor and the termination of processing when such detection is made.

Marshall teaches:

said processing unit stops said processing when said processing unit determines that said second data is not normal (Columns 8 and 9, Lines 63-67 and 1, respectively).

The motivation behind Marshall's teachings is to provide lockstep processors the opportunity to resolve errors inputted to these processors. Whether experienced by one or all of the processors, the end result could be a "lack of synchronization" where "the only recovery action would be to reset the system" (Column 2, Lines 4-6).

Accordingly, it would have been obvious to a person of ordinary skill in the art to affix the claimed command input circuit to a processor so that the processor may terminate processing based upon faulty input as described by Marshall so that it may receive commands at a faster rate.

Regarding Claim 11, Marshall teaches:

said processing unit stops said processing when said processing unit determines that one of said second to mth pieces of data is not normal (Columns 8 and 9, Lines 63-67 and 1, respectively).

8. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dreps in view of Suzuki.

Regarding Claim 5, Dreps does not disclose:

A processing unit going into a predetermined operation mode due to the second pieces of data.

Suzuki teaches:

said processing unit goes into a predetermined operation mode corresponding to said second command when the processing unit receives the second command (Figure 3; Column 7, Lines 3-7).

Suzuki states one of his goals in his teachings is to "accept a signal at high speed in order to retain an operation cycle at high speed" (Column 2, Lines 29-31).

It would have been obvious to a person of ordinary skill in the art at the time of invention to design the processor described by Dreps to incorporate the fast operation mode decision method system described by Suzuki for the benefit of allowing the data transfer system to quickly decide upon an operation mode and thus maximize the throughput of the system.

Regarding Claim 12, Suzuki teaches:

said processing unit goes into a predetermined operation mode corresponding to one of said second to mth commands when the processing unit receives said one of said second to mth commands (Figure 3; Column 7, Lines 3-7).

Allowable Subject Matter

9. Claims 13 and 15 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew A. Henry whose telephone number is (571) 272-3845. The examiner can normally be reached on Monday - Friday (8:00 am -5:00 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MAH

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